CLAIMS

WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising a ROM area and a RAM area both including memory cells each having a ferroelectric capacitor, wherein said ROM area comprises:

at least one real memory cell for storing data to be written in manufacturing process of said ferroelectric memory;

a dummy memory cell;

a reference memory cell having a ferroelectric capacitor therein whose residual dielectric polarization value is set to a predetermined value in the manufacturing process;

a first bit line connected to said real memory cell and said dummy memory cell, and transferring therethrough an electric charge corresponding to a residual dielectric polarization value of the ferroelectric capacitor which is included in a selected one of said real memory cell and dummy memory cell;

a second bit line connected to said reference memory cell, and transferring therethrough an electric charge corresponding to a residual dielectric polarization value of the ferroelectric capacitor which is included in said reference memory cell being selected in synchronization with a selection of said real memory cell or said dummy memory cell; and

a sense amplifier connected to said first and second bit lines, for amplifying a difference in voltage between said first and second bit lines, the difference occurring due to the transferred electric charges.

2. The ferroelectric memory according to claim 1, wherein

said first bit line connects a plurality of real memory cells.

3. The ferroelectric memory according to claim 1, further comprising:

first, second, and third word lines connected to said real memory cell, said dummy memory cell, and said reference memory cell, respectively, to select said real memory cell,

said dummy memory cell, and said reference memory cell; and

first, second, and third plate lines connected to said real memory cell, said dummy memory cell, and said reference memory cell, respectively, wherein

said first to third word lines and said first to third plate lines are wired in a same direction.

4. The ferroelectric memory according to claim 1, further comprising:

first, second, and third word lines connected to said real memory cell, said dummy memory cell, and said reference memory cell, respectively, to select said real memory cell, said dummy memory cell, and said reference memory cell; and

first, second, and third plate lines connected to said real memory cell, said dummy memory cell, and said reference memory cell, respectively, wherein

said first to third word lines are wired orthogonally to said first to third plate lines.

5. The ferroelectric memory according to claim 1, wherein said RAM area comprises:

normal memory cells for reading data therefrom and writing data thereto; and

a reference memory cell used in accessing said normal memory cells, wherein

a size of said ferroelectric capacitor of said reference memory cell in said ROM area is larger than a size of a ferroelectric capacitor of said reference memory cell in said RAM area.

6. The ferroelectric memory according to claim 1, wherein

the data written into said real memory cell in advance is authentication data.

7. The ferroelectric memory according to claim 6, wherein

said authentication data is key data used in the Public Key Infrastructure.

8. A method of reading data in a ferroelectric memory comprising a ROM area and a RAM area both including memory cells each having a ferroelectric capacitor, said ROM area comprising: a first bit line connected to a dummy memory cell and a real memory cell, said

real memory cell storing therein data to be written in manufacturing process; a second bit line connected to a reference memory cell having a ferroelectric capacitor which is included in reference memory cell whose residual dielectric polarization value is set to a predetermined value in the manufacturing process; and a sense amplifier connected to said first and second bit lines, for amplifying a difference in voltage between said first and second bit lines, said difference occurring due to the transferred electric charges, the method comprising the step of:

executing, prior to a first read operation for reading real data from said real memory cell, a second read operation for reading dummy data from said dummy memory cell.

9. The method of reading data in a ferroelectric memory according to claim 8, wherein: said first read operation comprises the steps of

selecting said real memory cell and said reference memory cell,

transferring electric charges corresponding to residual dielectric polarization values of said real memory cell and of said reference memory cell to said first and second bit lines, respectively, and

operating said sense amplifier; and

said second read operation comprises the steps of

selecting said dummy memory cell and said reference memory cell,

transferring electric charges corresponding to residual dielectric polarization values of said dummy memory cell and of said reference memory cell to said first and second bit lines, respectively, and

operating said sense amplifier.

10. The method of reading data in a ferroelectric memory according to claim 8, further comprising the steps of:

executing said second read operation as an initial read operation after power-on of said ferroelectric memory; and

executing said first read operation as at least one of second and subsequent read operations.

11. The method of reading data in a ferroelectric memory according to claim 10, further comprising the step of:

successively executing said second read operation and said first read operation after the power-on.

12. The method of reading data in a ferroelectric memory according to claim 8, wherein the data written into said real memory cell in advance is authentication data.

13. The method of reading data in a ferroelectric memory according to claim 12, wherein

said authentication data is key data used in the Public Key Infrastructure.